IN THE CLAIMS:

Please amend claims 1, 4-5, 9-10, 14 and 17-18 as follows:

1. (Currently Amended) A video signal processing system for processing video data and graphic data, comprising:

a) a filter unit, which receives the video data, and horizontally and vertically filters the video data to convert the video data into video pictures formatted with a different number of columns and/or lines, and provides a filtered video signal indicative thereof, where the filter unit buffers individual pixels and/or lines in a first memory;

b) a second memory that receives and stores the graphic data and the filtered video signal and provides stored signals indicative thereof;

c) a third memory that is connected to the second memory, and stores data received from the second memory ~~devices~~; and

d) a mixing unit that receives and mixes the stored graphic data and the stored filtered video data to provide a video output signal.

2. (Previously Presented) The video signal processing system of claim 1, where the first memory comprises random access memory.

3. (Previously Presented) The video signal processing system of claim 1, where the second memory is configured as cache memory.

4. (Currently Amended) The video signal processing system of claim 1, where the third memory ~~device~~ comprises random access memory.

5. (Currently Amended) The video signal processing system of claim 1, where the graphic

~~graphic~~ data comprises bitmaps received from a processor.

6. (Previously Presented) The video signal processing system of claim 1, comprising:

a controller that controls the filter unit, the first, second and third memories and the mixing unit to control the processing of the video signal procesing system.

7. (Previously Presented) The video signal processing system of claim 6, where the video signal processing system operates in real time with the clock frequency of the controller being higher than the clock frequency of the signal associated with the video data and the video output signal.

8. (Previously Presented) The video signal processing system of claim 6, where the controller comprises a processor.

9. (Currently Amended) A video signal processing system for processing video data and graphic data, comprising:

a) a horizontal filter that receives and converts the video data into video pictures formatted with a different number of columns, and provides a horizontally filtered video signal indicative thereof, where the horizontal filter buffers individual pixels and/or lines in a first memory;

b) a second memory that receives and stores the graphic data and the horizontal filtered video signal and provides stored signals indicative thereof;

c) a third memory that is connected to the second memory, and stores data received from the second memory; and

d) a mixing and filtering unit that receives the stored graphic data and the stored horizontally

filtered video data, vertically filters the stored horizontally filtered video data to convert the video data into video pictures with a different number of lines and provide a vertically filtered signal indicative thereof, and mixes the stored graphic data with the vertically filtered video signal to provide a video output signal.

10. (Currently Amended)The video signal processing system of claim 9, where the second memory ~~device~~ is configured as a cache memory.

11. (Previously Presented) The video signal processing system of claim 9, where the third memory comprises random access memory.

12. (Previously Presented) The video signal processing system of claim 9, where the graphic data comprises bitmaps received from a processor.

13. (Previously Presented) The video signal processing system of claim 9, comprising:

a controller that controls the horizontal filter, the first, second and third memories and the mixing unit to control the processing of the video signal procesing system.

14. (Currently Amended) The video signal processing system of claim 13, where the clock frequency of the controller is higher than the clock frequency of a signal at the video input signal and the video output signal.

15. (Previously Presented) The video signal processing system of claim 14, where the controller

comprises a processor.

16. (Previously Presented) The video signal processing system of claim 9, where the video signal processing system is used for interlace progressive conversion.

17. (Currently Amended) A video signal processing system for processing a video data and graphic data, comprising:

a filter unit, which receives the video data and filters the video data to convert the video data into video pictures formatted with a different number of columns and/or lines, and provides a filtered video signal indicative thereof, where the filter unit buffers individual pixels and/or lines in a first memory;

~~b)~~ a second memory that receives and stores the graphic data and the filtered video signal and provides stored signals indicative thereof;

~~c)~~ a third memory that is connected to the second memory, and stores data received from the second memory device; and

~~d)~~ a mixing unit that receives and mixes the stored graphic data and the stored filtered video data to provide a video output signal.

18. (Currently Amended) A video signal processing system for processing a video data and graphic data, comprising:

a) a horizontal filter that receives and converts the video data into video pictures formatted with a different number of columns, and provides a horizontally filtered video signal indicative thereof, where the horizontal filter buffers individual pixels and/or lines in a first memory;

b) a second memory that receives and stores the graphic data and the filtered video signal and provides stored signals indicative thereof;

c) a third memory that is connected to the second memory, and stores data received from the second memory; and

d) a mixing and filtering unit that receives the stored graphic data and the stored horizontally filtered video data, vertically filters the stored horizontally filtered video data to convert the video data into video pictures with a different number of lines and provide a vertically filtered signal indicative thereof, and mixes the stored graphic data with the vertically filtered video signal to provide a video output signal.